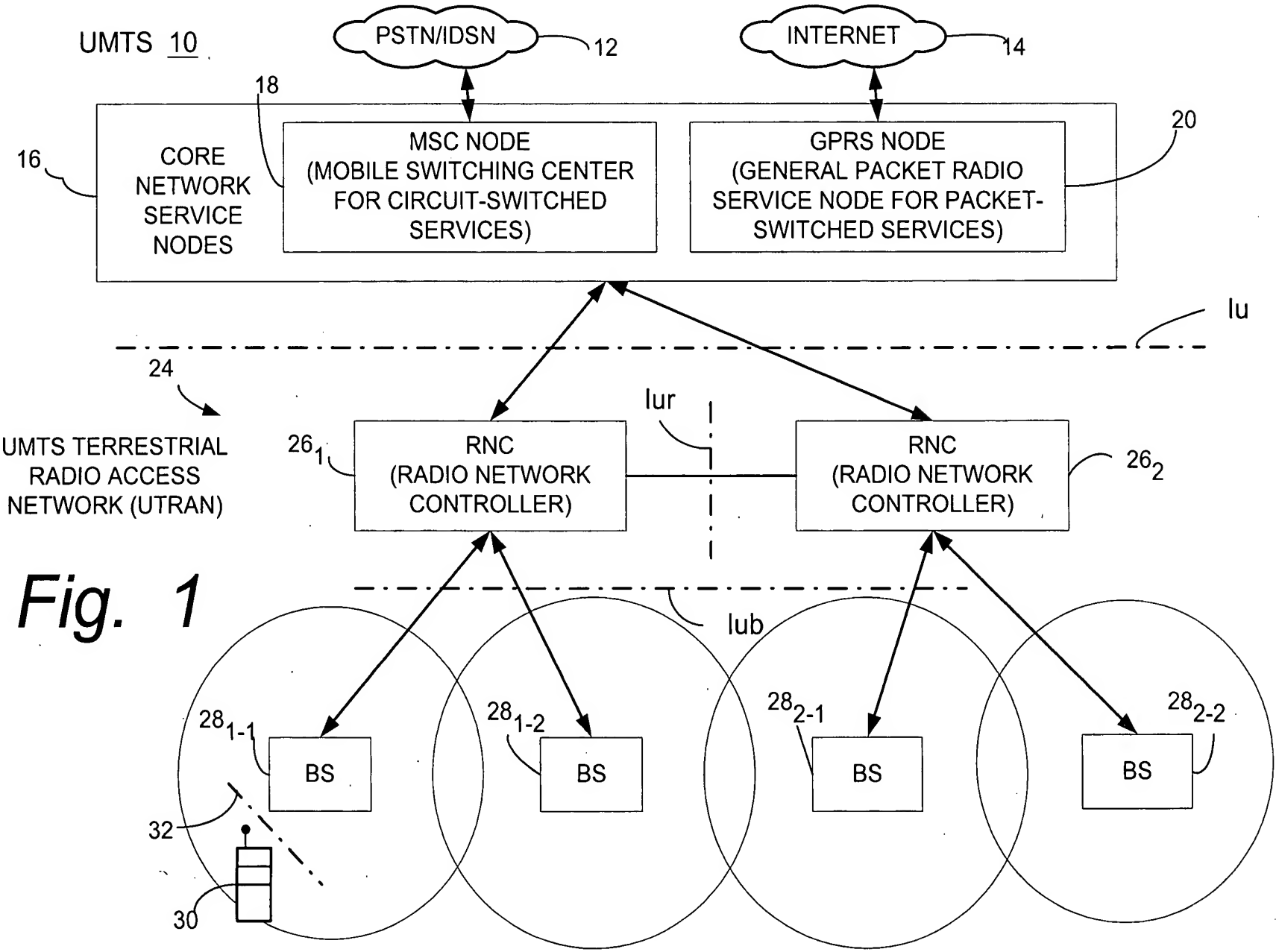

Fig. 1

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2/16
20sfp0 - 4n20sh0ot

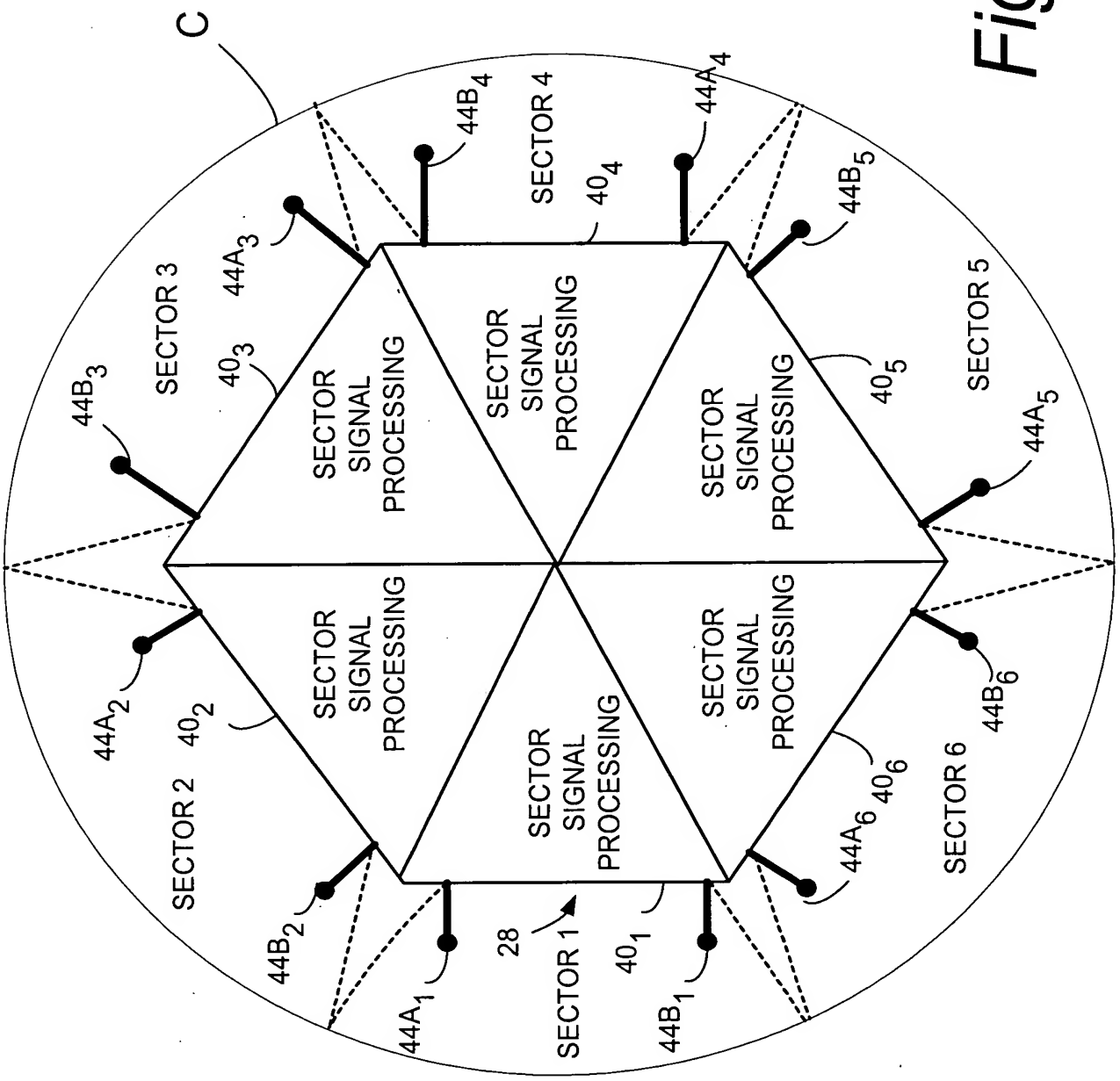


Fig. 2

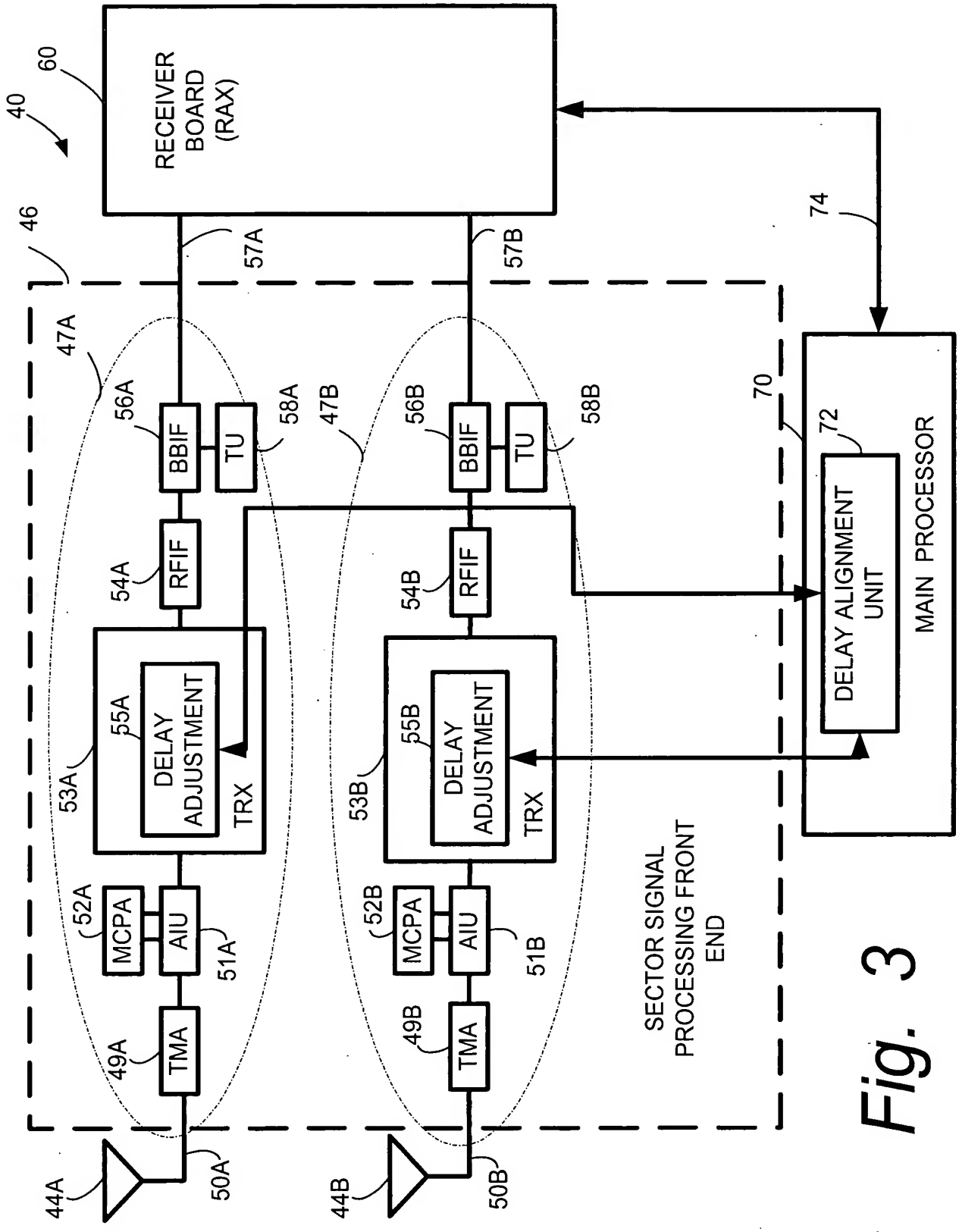

40
60
RECEIVER BOARD (RAX)
46
57A
57B
74
47A
47B
56A
56B
BBIF
TU
58A
58B
54A
54B
RFIF
70
72
DELAY ALIGNMENT UNIT
MAIN PROCESSOR
53A
53B
55A
55B
DELAY ADJUSTMENT
TRX
52A
52B
MCPA
AIU
51A
51B
49A
49B
TMA
SECTOR SIGNAL PROCESSING FRONT END
44A
44B
50A
50B

Fig. 3

20STF0" h20shoot

Fig. 4

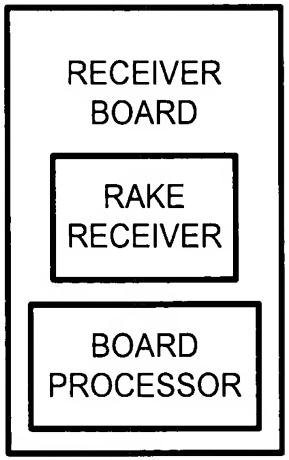
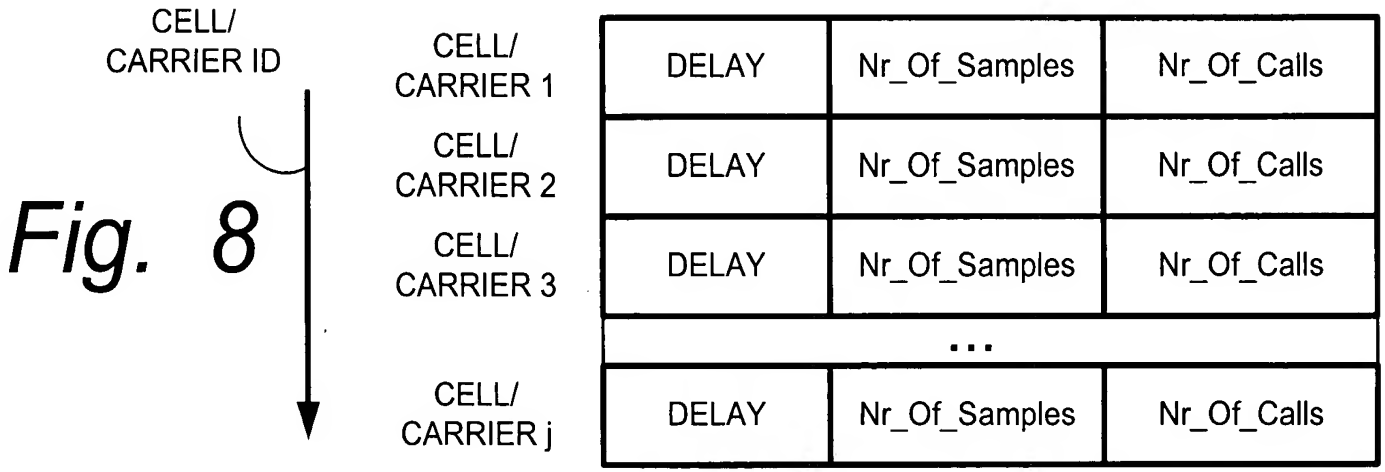


Fig. 8



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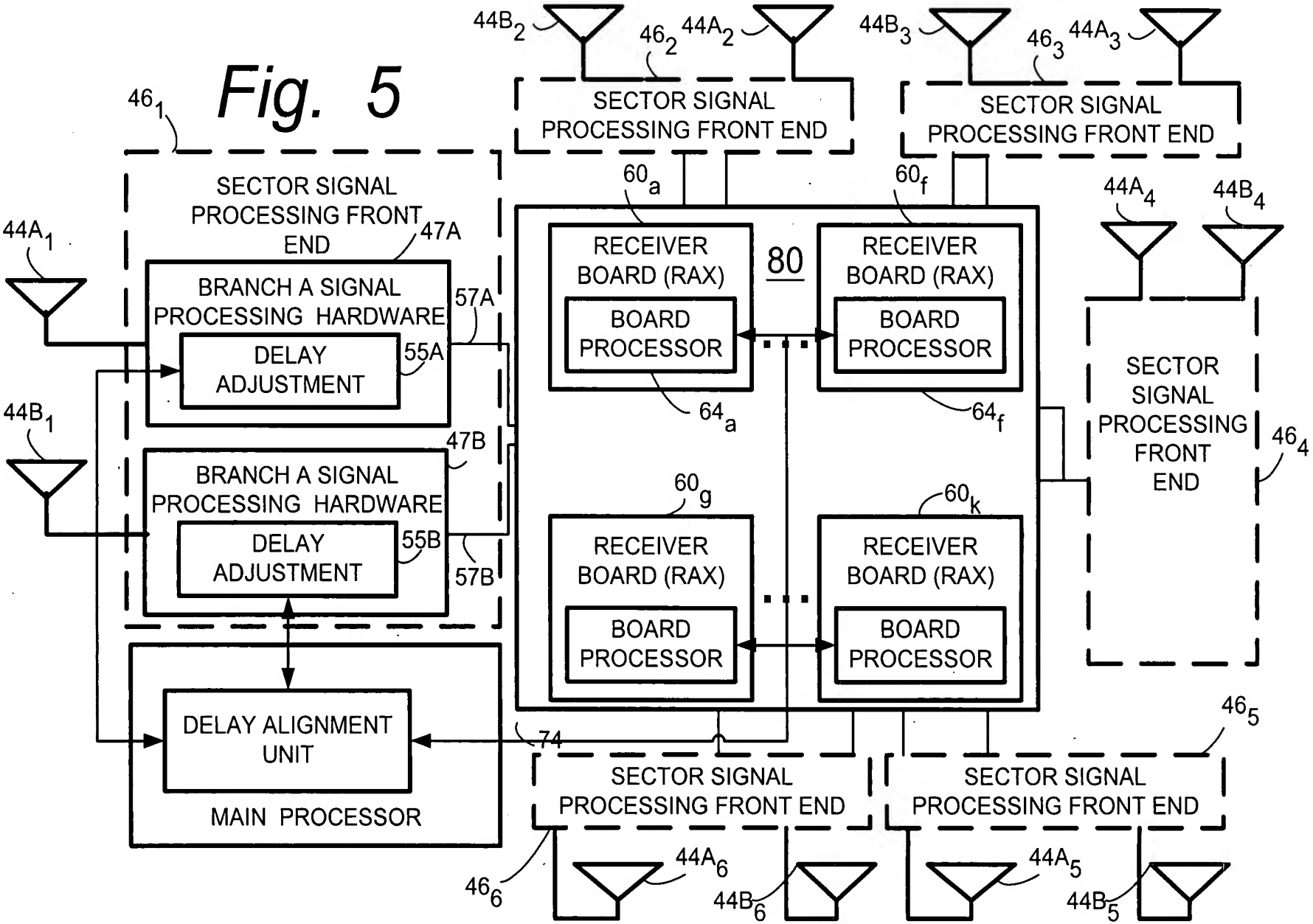
20STTO" h20Shoot

Fig. 5



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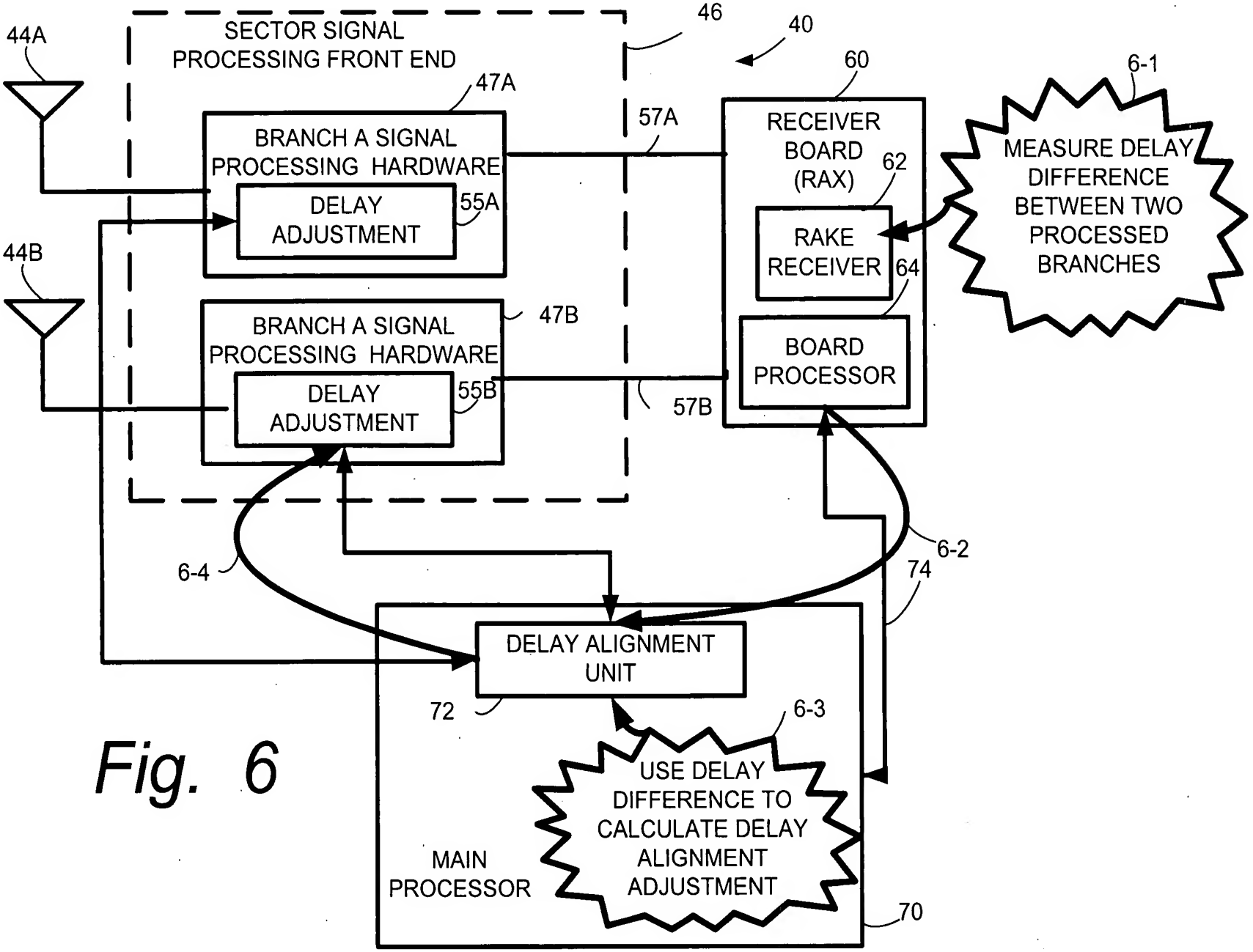

Fig. 6

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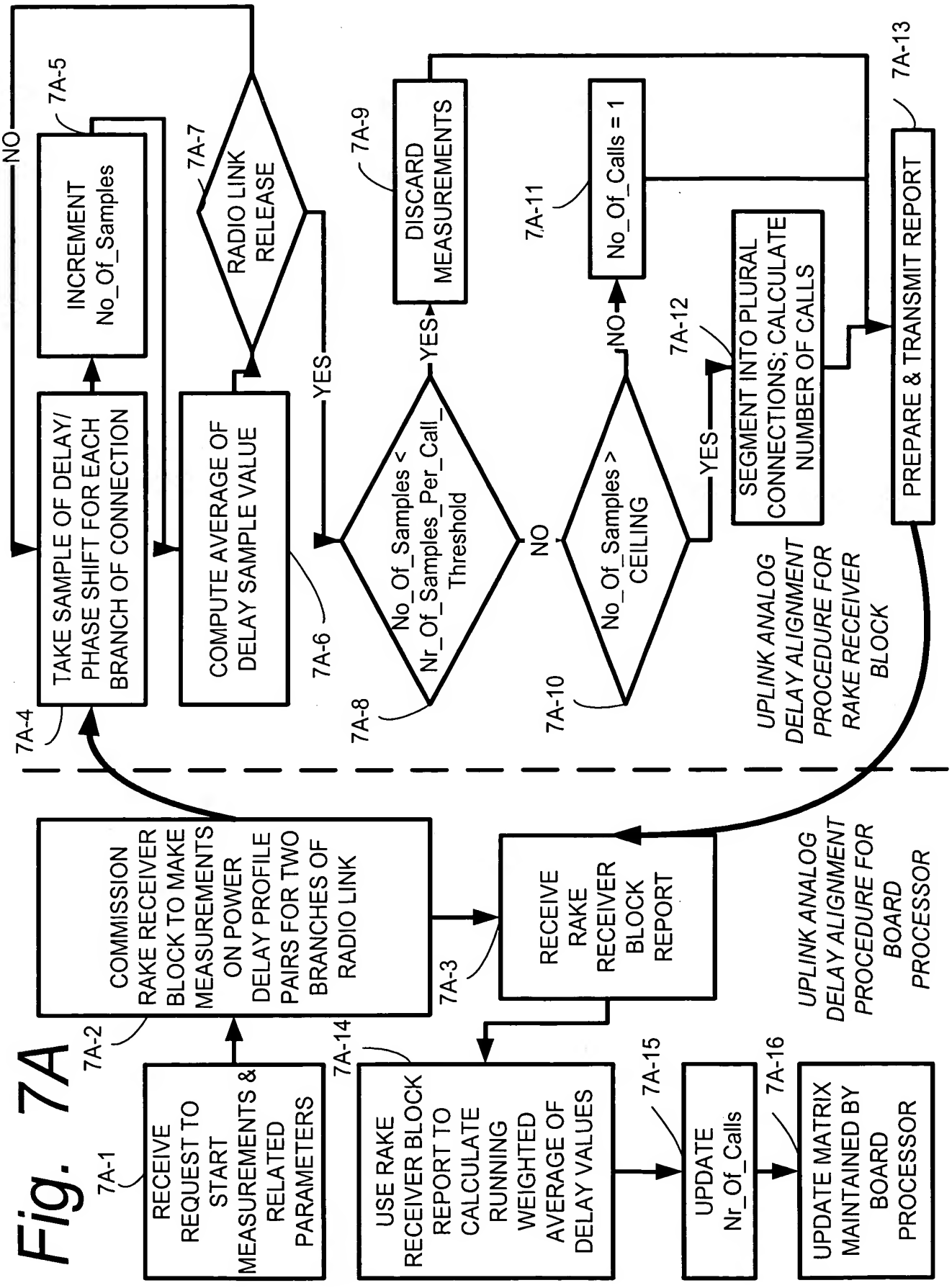
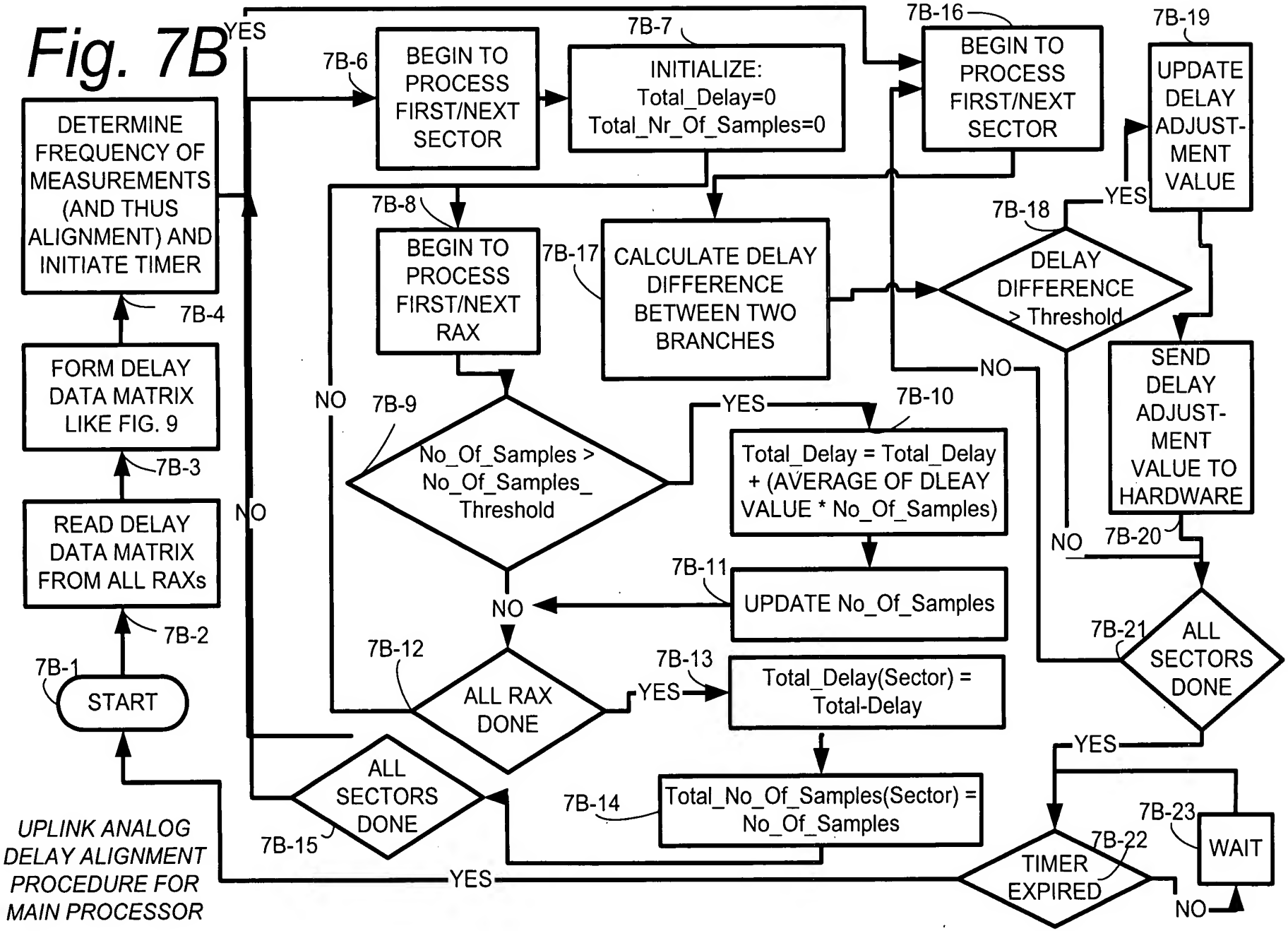
20STEP "h2O5hOOT

Fig. 7A



20STTO" h20ShOOT

Fig. 7B



UPLINK ANALOG DELAY ALIGNMENT PROCEDURE FOR MAIN PROCESSOR

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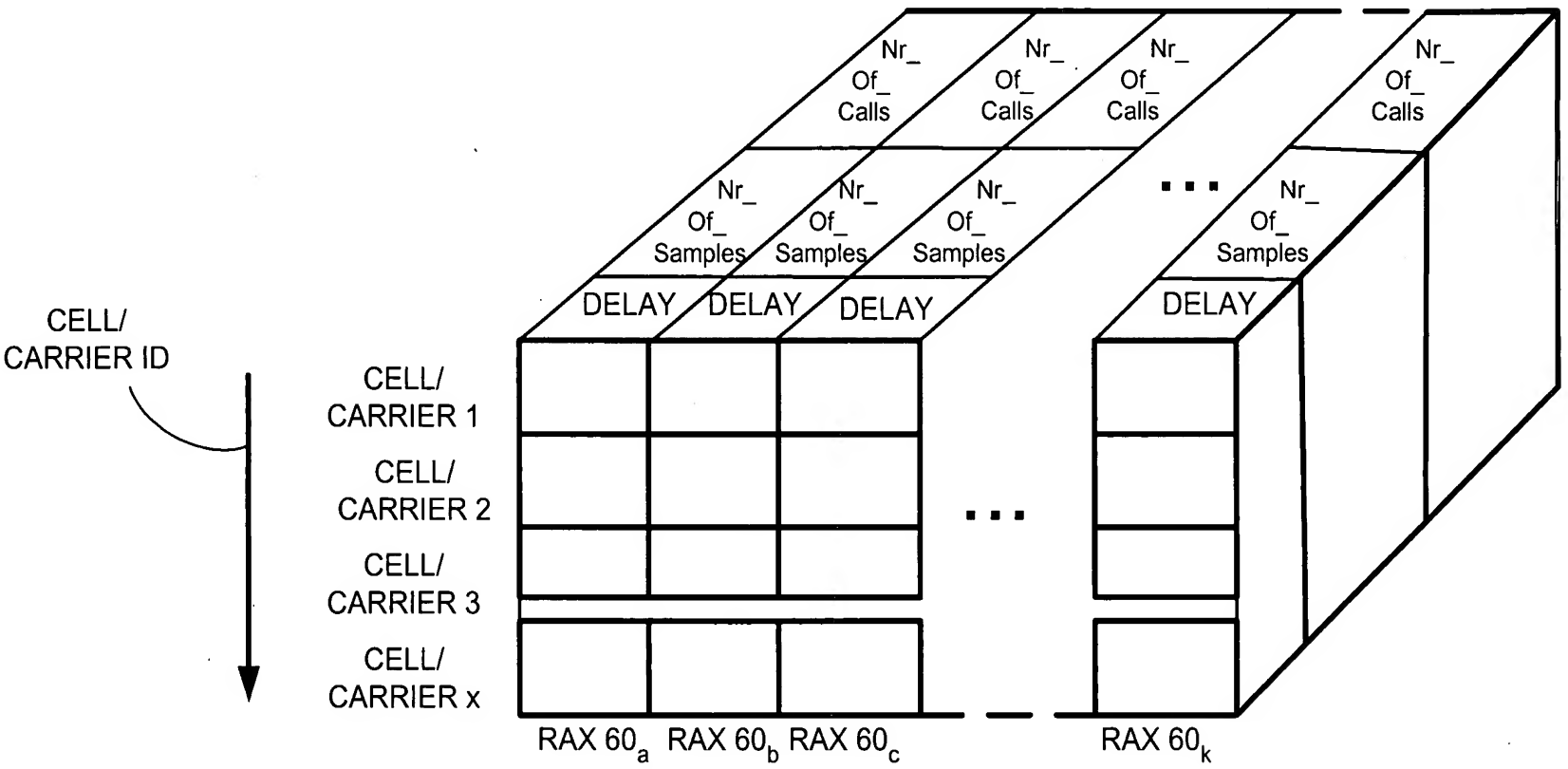

Fig. 9

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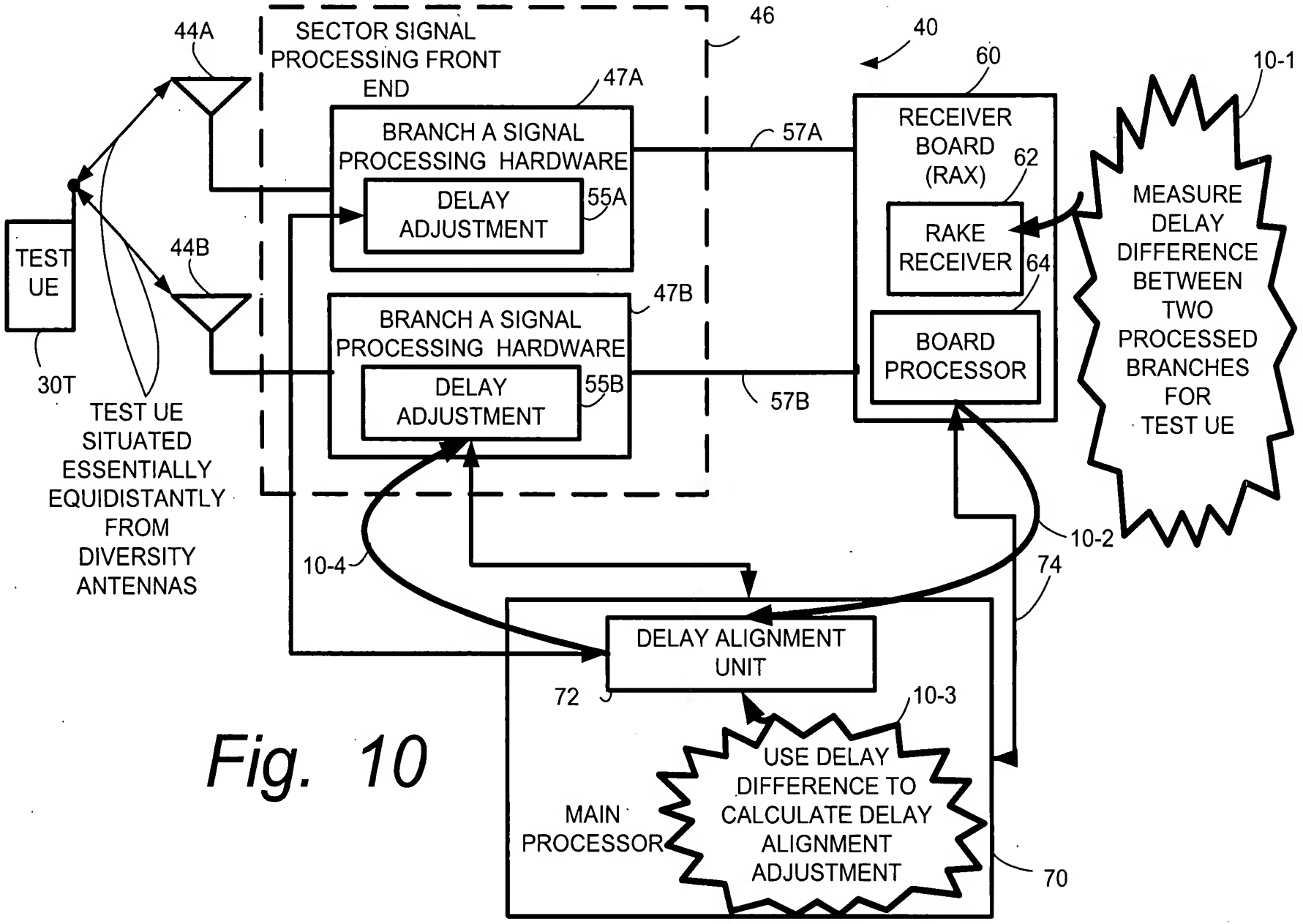

Fig. 10

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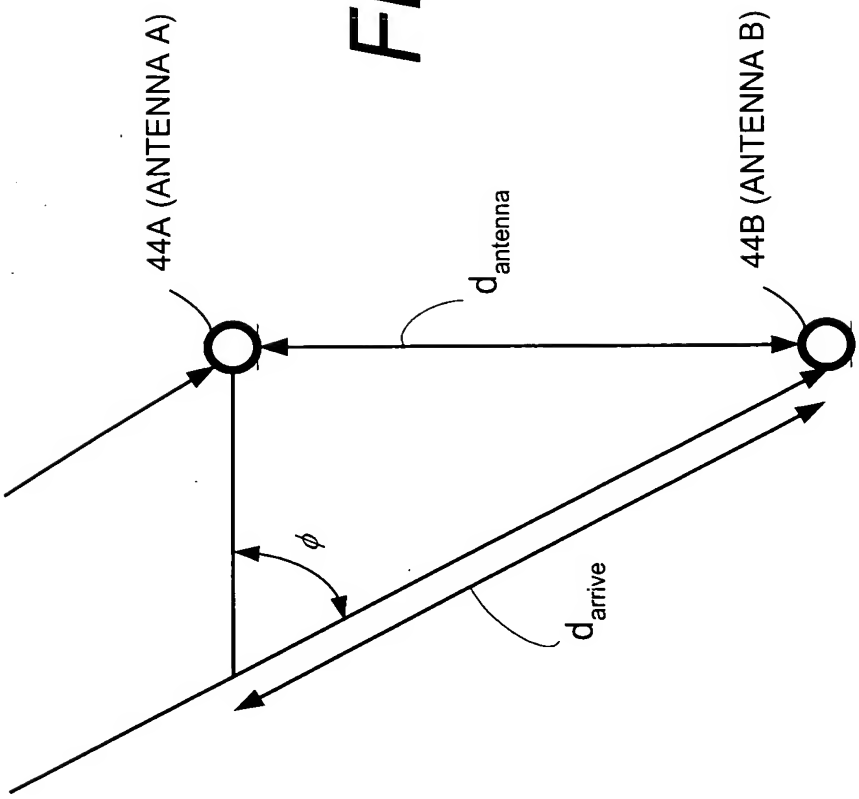
Fig. 11



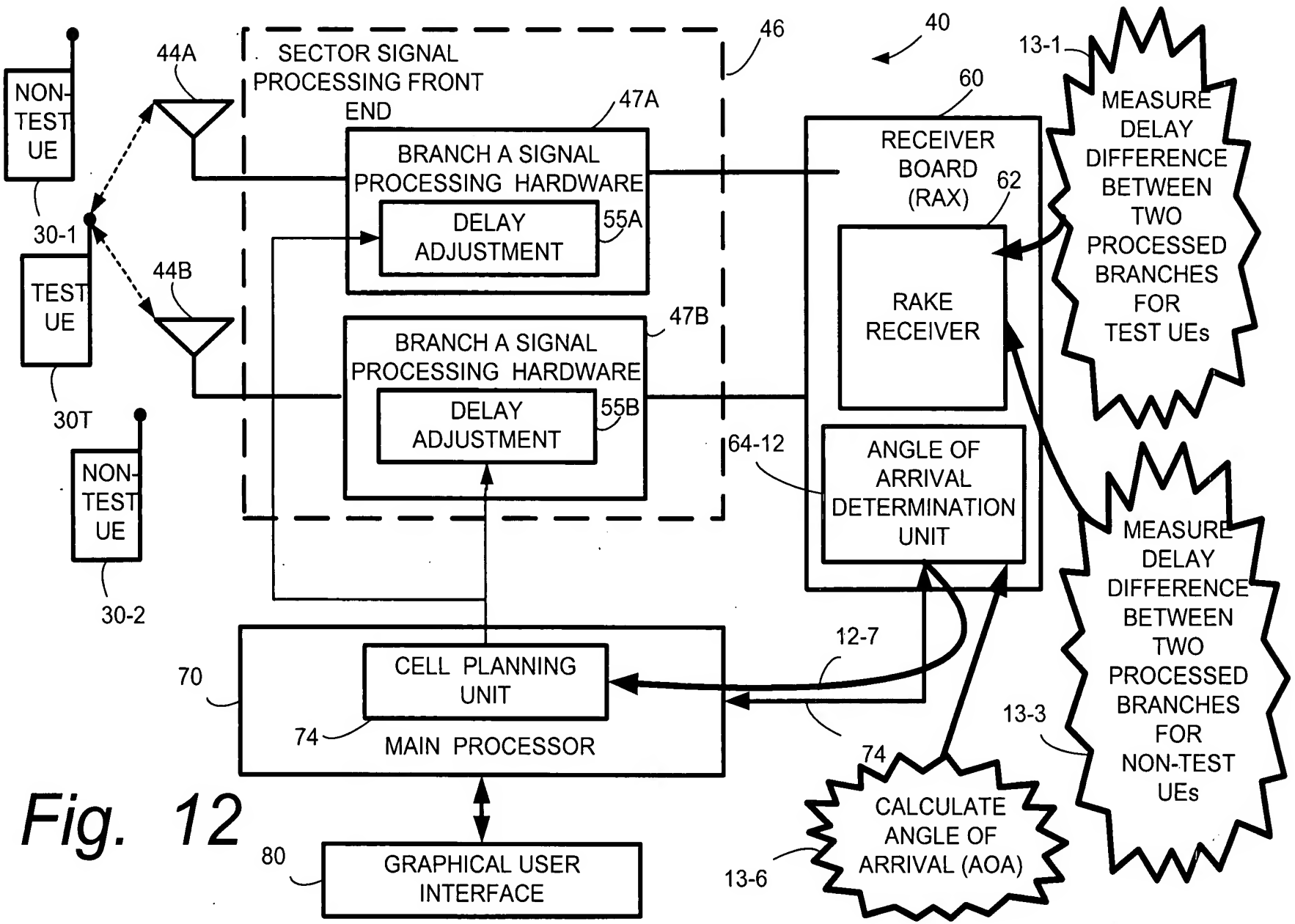


Fig. 12

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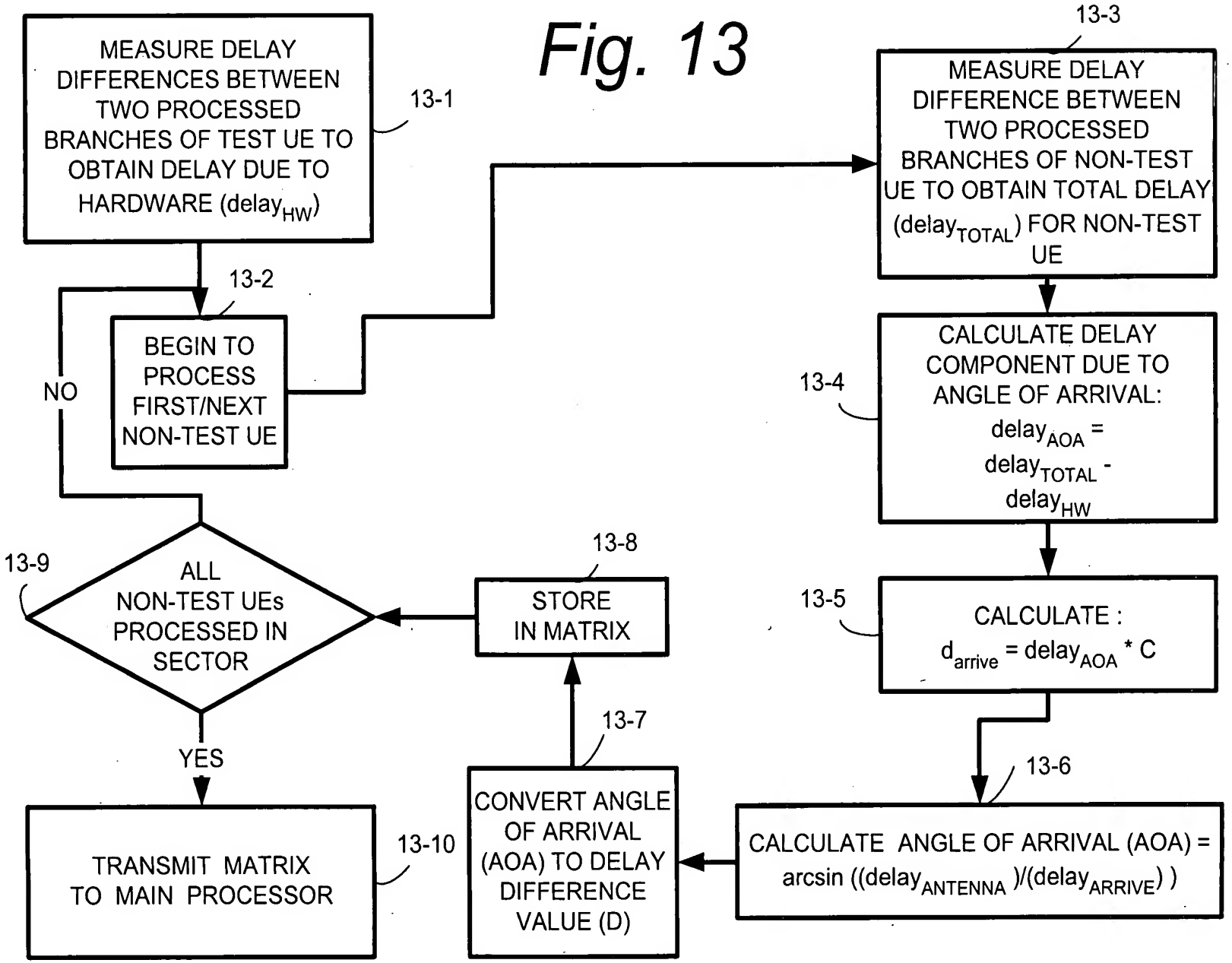
20STTO"h20ShOOT

Fig. 13



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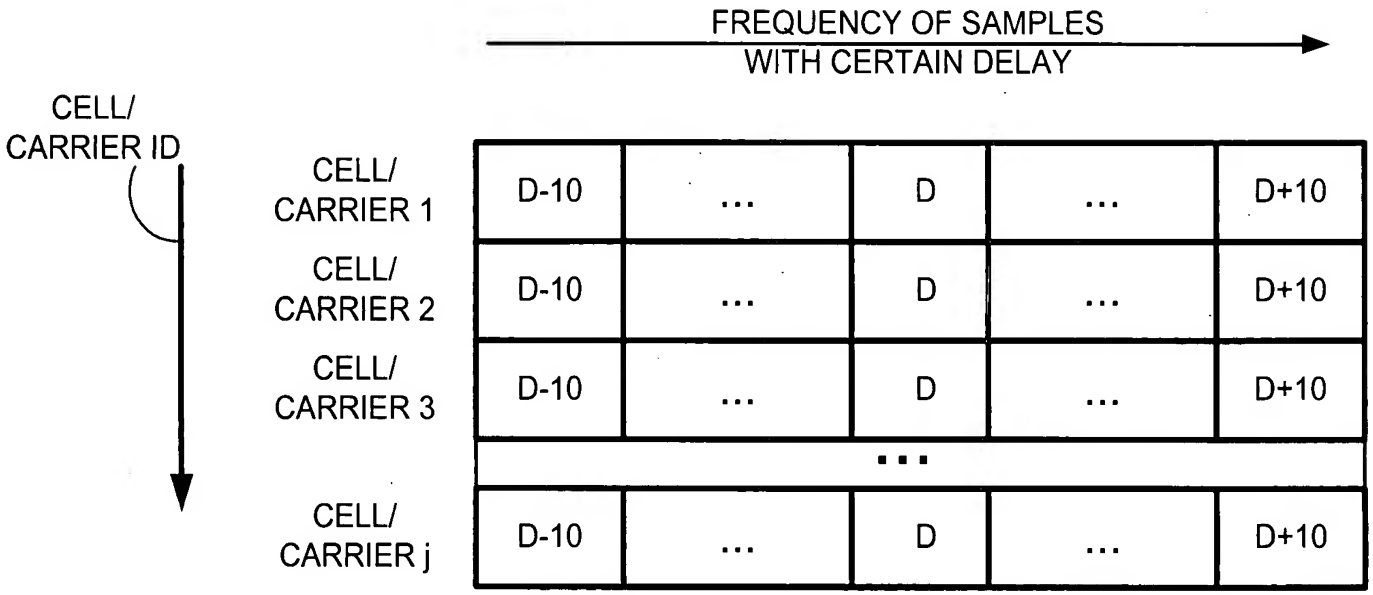

Fig. 14

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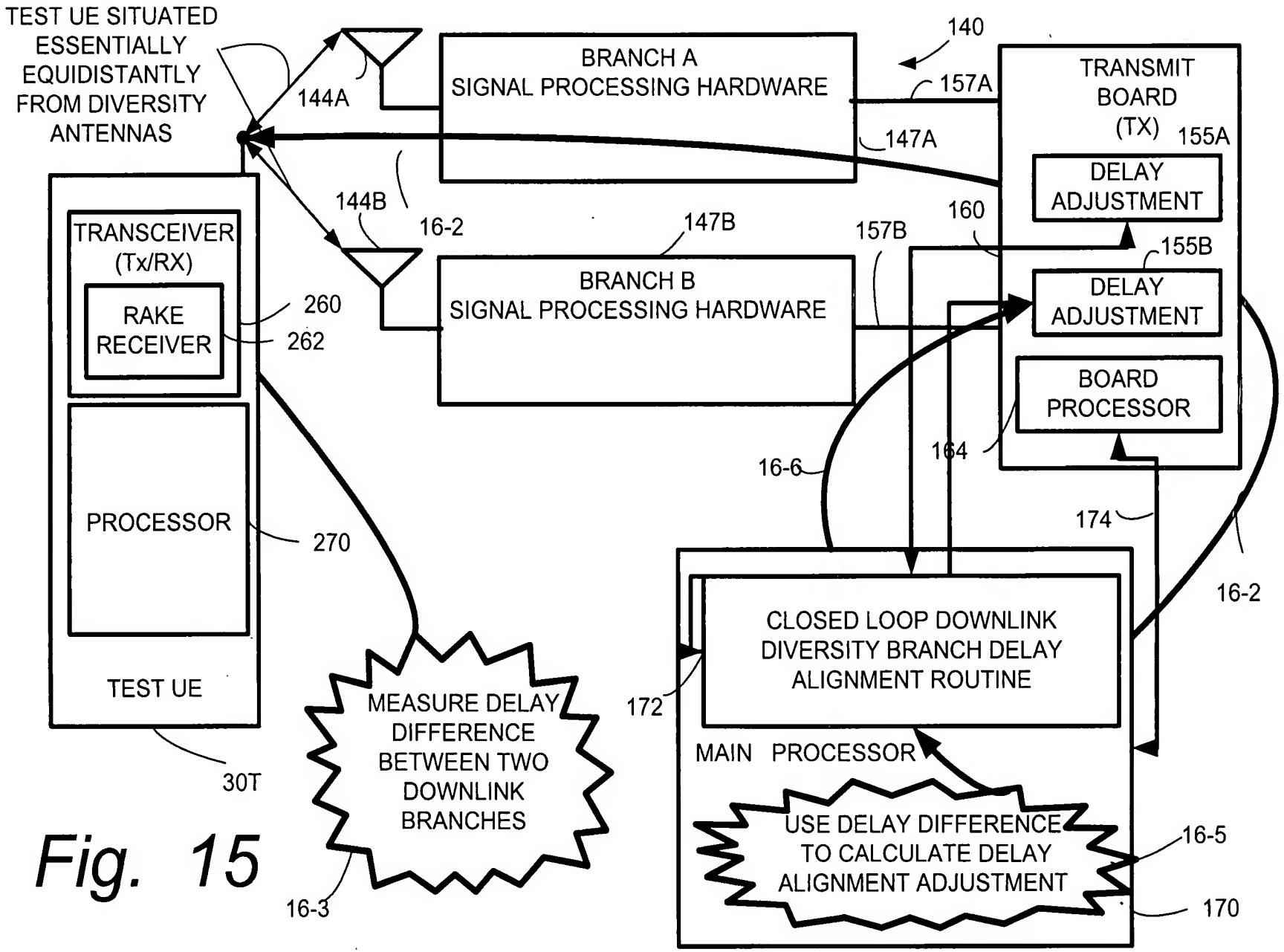

Fig. 15

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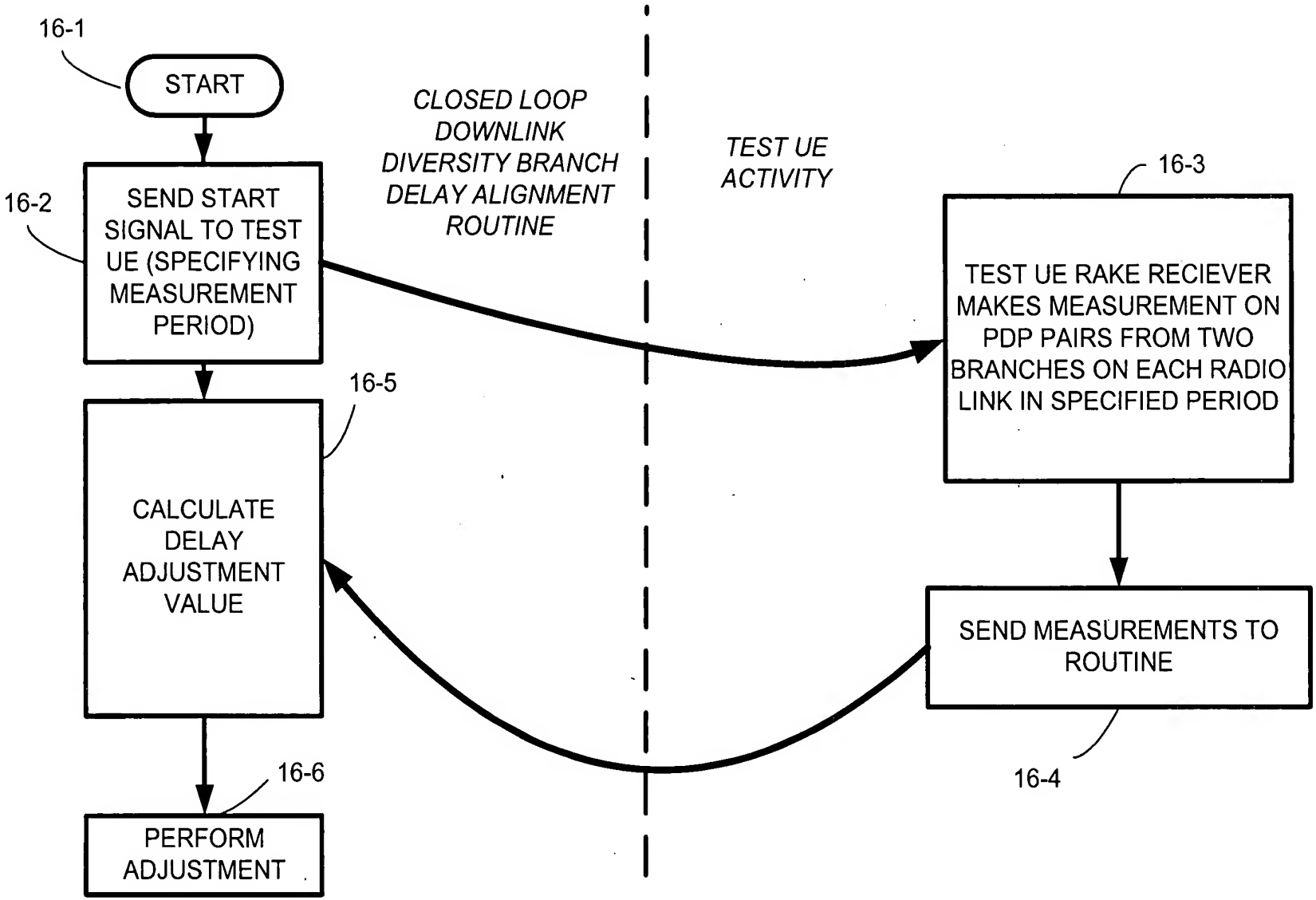

Fig. 16

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